EXHIBIT A

(Decision After Director Remand)

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Paper 19
Entered: July 20, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WOLFSPEED, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00761
Patent 7,498,633 B2

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI, and JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION AFTER DIRECTOR REMAND
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Wolfspeed, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") for *inter partes* review of claims 9–11 of U.S. Patent No. 7,498,633 B2 (Ex. 1001, "the '633 patent"). The Trustees of Purdue University ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With Board pre-authorization, Petitioner filed a Preliminary Reply (Paper 7) and Patent Owner filed a Preliminary Sur-reply (Paper 8) limited to addressing Patent Owner's request that the Board exercise its discretion and deny the Petition under 35 U.S.C. § 325(d). *See* Ex. 1024 (authorization).

We previously entered a decision in which we exercised our discretion and denied review pursuant to § 325(d). Paper 9 ("the Board's Decision"). The Director thereafter entered a decision that vacated the Board's Decision and remanded for further proceedings. Paper 13 ("the Director's Decision").

A. Real Parties-in-Interest

The Petition identifies "Wolfspeed" as the sole "real party-in-interest" for Petitioner. Pet. 5. Patent Owner's Mandatory Notice identifies "[t]he Trustees of Purdue University and the Purdue Research Foundation" as real parties-in-interest for Patent Owner. Paper 3, 1.

B. Related Matters

Both parties identify as related matters the co-pending district court actions in *The Trustees of Purdue University v. STMicroelectronics N.V. et al.*, No. 6:21-cv-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-cv-840 (M.D.N.C.). Pet. 5; Paper 3, 1. Both parties also identify as a related matter a prior Board proceeding in

IPR2022-00252 ("IPR252"). Pet. 5; Paper 3, 1. Patent Owner, but not Petitioner, also identifies IPR2022-00723. Pet. 5; Paper 3, 1.

C. Procedural History

On November 8, 2022, we entered the Board's Decision that denied Petitioner's request for *inter partes* review based on a determination that the Petition "raises substantially the same prior art previously presented to the Board in IPR252" and does not establish reversible error in the decision entered in that prior proceeding. Paper 9, 15. We did not reach the questions of whether (1) the Petition raises the same or substantially the same arguments previously presented to the Board in IPR252, or (2), on the merits, the patentability challenges advanced in the Petition satisfy the reasonable likelihood of prevailing standard necessary to support institution of an *inter partes* review under § 314(a).

Petitioner filed a request for rehearing of the Board's Decision on December 8, 2022. Paper 10. On December 13, 2022, Petitioner filed a request for review by the Precedential Opinion Panel ("POP"). Ex. 3001. On March 30, 2023, the Director *sua sponte* issued a decision that granted Director review, vacated the Board's Decision, and remanded the case to the Board for further proceedings. Paper 13 ("the Director's Decision"). In particular, the Director determined that the prior art asserted in the instant Petition is not substantially the same as the prior art that previously was asserted in IPR252, because the art asserted in this proceeding teaches a "transistor topology" that "would *not* compromise ruggedness." *Id*. at 8. That same day, on March 30, 2023, a panel that included the Director issued an Order dismissing Petitioner's request for POP review. Paper 14.

On April 5, 2023, the Board issued an Order explaining "that a decision on institution will issue as soon as possible and, in any event, no later than September 29, 2023." Paper 15, 2. Two days later, on April 7, 2023, Patent Owner filed a request for rehearing of the Director's Decision. Paper 16. On April 13, 2023, the Director ordered "a temporary stay of the underlying proceeding pending [the Director's] decision on Patent Owner's rehearing request." Paper 17, 2. On May 4, 2023, the Director lifted the stay and denied Patent Owner's rehearing request with instructions "that the Board shall not decide" that request. Paper 18, 2.

Jurisdiction now returns to the Board to resolve Petitioner's request for *inter partes* review in a manner consistent with the Director's Decision. In this Decision, we execute the Director's instructions that the Board "reassess its § 325(d) analysis consistent with" the Director's Decision and, "[i]f the Board determines that it should not exercise its discretion to deny institution of *inter partes* review under § 325(d), then the Board should address the remaining issues raised in the Petition and Preliminary Response to determine whether to institute an *inter partes* review." Paper 13, 3.

II. BACKGROUND

A. The '633 Patent (Ex. 1001)

The '633 patent is titled "High-Voltage Power Semiconductor Device." Ex. 1001, code (54). The '633 patent relates to a double-implanted metal-oxide semiconductor field effect transistor ("DIMOSFET") having a substrate, a drift layer formed on the substrate, first and second source regions, and a junction field-effect transistor ("JFET") region defined between the first and second source regions. *Id*. at code (57). The technical

field of the invention is power MOSFETs, that is, MOSFETs suitable for use in "high-voltage power applications." *Id.* at 1:14–20.

The DIMOSFET of the claimed invention includes a "first source electrode formed over the first source region, the first source electrode defining a longitudinal axis" and "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode." *Id.* at 9:47–53 (claim 9). Similarly, the DIMOSFET includes a second source electrode formed over the first source region and a plurality of second base contact regions spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode. *Id.* at 9:55–10:5.

The specified semiconductor device also includes a JFET region located between the first source region and the second source region and, in some embodiments, the JFET region has "a width less than about three micrometers." *Id.* at 10:6–8 (claim 9).

The base contact regions may be "embodied as small 'islands' or regions within the larger source regions." *Id.* at 7:57–59. Such a configuration is illustrated in Figure 3, which we reproduce below.

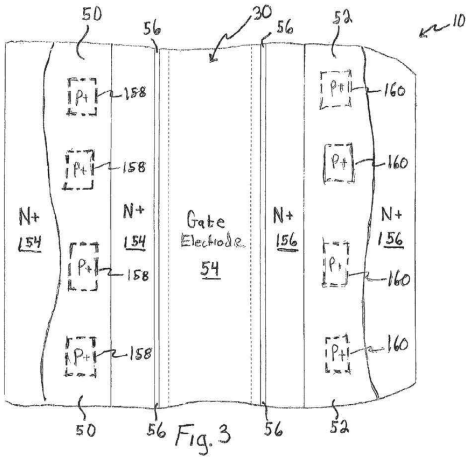
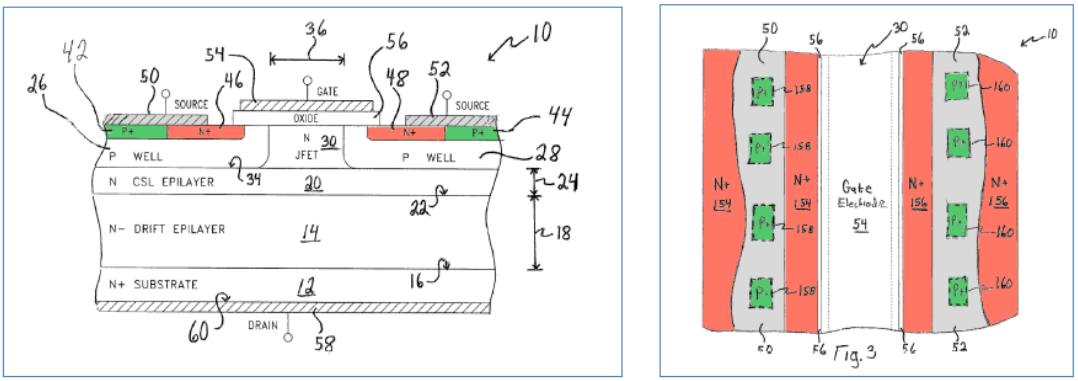


Fig. 3

Ex. 1001, Fig. 3. Figure 3 is a plan view of semiconductor 10, an embodiment of the invention according to the '633 patent. *Id*. at 3:54–55. Semiconductor 10 includes p+ base contact regions 158 and 160, which are "embodied as small 'islands' or regions within" larger n+ source regions 154 and 156.[1] *Id*. at 7:57–59.

The p+ base contact regions "are formed to be located in a central location under" source electrodes 50, 52, with areas of the n+ source regions "spaced between each" p+ base contact region. *Id*. at 7:59–63. The outer edges of source electrodes 50, 52 are removed in Figure 3 "for clarity." *Id*. at 7:64–65. The relative locations of those elements are shown in Petitioner's side-by-side comparison of Figures 1 and 3, reproduced below.



Pet. 23 (reproducing Ex. 1001, Figs. 1, 3, with annotations supplied by Petitioner). The above illustration is a side-by-side comparison of Figure 1 (cross-sectional view) on the left and Figure 3 (plan view) on the right. Ex. 1001, 3:52–57. Petitioner highlights in red the n+ source regions, in green the p+ base contact regions, and in gray source electrodes 50, 52.

[1] P+ and p+ both refer to semiconductor areas doped p-type, whereas N+ and n+ both refer to semiconductor areas doped n-type.

B. Challenged Claims

We reproduce below independent claim 9.

> 9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
>
> a silicon-carbide substrate;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
>
> a first source region;
>
> a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
>
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
>
> a second source region;
>
> a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
>
> a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
>
> a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Ex. 1001, 9:41–10:8. Claims 10 and 11 depend from claim 9 and, thereby, inherit each limitation of claim 9. Claims 10 and 11 add additional limitations that relate to the JFET region width (claim 10) or the relative degree of concentrations of impurities as between the JFET region and the drift semiconductor layer (claim 11). *Id.* at 10:9–18.

C. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 9–11 on two grounds:

Ground	35 U.S.C. §	Reference(s)
1	103[2]	Ryu[3] and Depetro[4]
2	103	Ryu and Choy[5]

Pet. 7. Petitioner relies on the Declaration of Jack Lee, Ph.D. (Ex. 1010).

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the art at the time of the invention is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

The parties dispute the level of ordinary skill in the art. *Compare* Pet. 29 (Petitioner's proposed definition), *with* Prelim. Resp. 15–18 (Patent Owner's opposition and proposed alternative definition). Neither party indicates, however, that resolution of that dispute is necessary to our decision whether to institute review.

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[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the '633 patent has an effective filing date before March 16, 2013 (Ex. 1001, codes (22), (60), (65)), we refer to the pre-AIA version of §103. Neither party indicates the result would change based on the version applied.

[3] U.S. Patent Application Publication No. 2004/0119076 A1, published June 24, 2004, filed October 30, 2003 (Ex. 1003).

[4] U.S. Patent No. 6,043,532, issued March 28, 2000 (Ex. 1004).

[5] U.S. Patent No. 5,171,705, issued Dec. 15, 1992 (Ex. 1005).

Based on the information presented, we find that the prior art demonstrates sufficiently the level of skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself can reflect the appropriate level of ordinary skill in the art). The following decision on institution does not depend on, or require, resolution of the dispute surrounding the level of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, the Board construes the terms of a patent claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under that standard, claim terms generally are given their plain and ordinary meaning as would have been understood by the ordinarily skilled artisan at the time of the invention and within the context of the entire patent disclosure. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

We construe terms in controversy only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Neither party indicates that an express construction for any claim term is necessary to our decision whether to institute review. Pet. 29–30; Prelim. Resp. 18. On this record, we determine that no claim term requires express construction for our purposes.

C. Principles of Law

We are authorized to institute an *inter partes* review only if the information presented in a petition and preliminary response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least [one] of the claims challenged in the petition." 35 U.S.C. § 314(a). We are never compelled to institute review, however, and § 325(d) provides the Director, and by delegation the Board, discretion to deny a petition that raises the same or substantially the same prior art or arguments previously presented to the Office. Under § 325(d), the Board "may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." In view of the Director's instructions, we limit our analysis under § 325(d) to whether the Petition raises the same or substantially the same arguments previously presented to the Office. Paper 13, 3.

The Petition is limited to challenges based on obviousness. Pet. 7 (grounds chart). A claim is obvious if the differences between the claimed subject matter and "the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

Several factual determinations underlie an obviousness analysis: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham*, 383 U.S. at 17–18. The inquiry includes an analysis of "whether there was an apparent reason to combine the known elements in the fashion

claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness").

In the analysis that follows, we first address whether the Petition raises the same or substantially the same arguments previously presented to the Office, and then turn to whether the information presented meets the evidentiary showing necessary to support institution under § 314(a). We are guided, on the second issue, by the statute and precedent instructing that Petitioner bears "the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)).

D. 35 U.S.C. § 325(d)

We first reassess our § 325(d) analysis, as instructed by the Director. Paper 13, 3. The question before us is whether the same or substantially the same arguments previously were presented to the Office in IPR252. *Id*. at 8–9. As the Director determined, Petitioner here asserts two references, Depetro and Choy, which are materially different from the references previously presented to the Office in IPR252. *Id*. at 7–8.

The arguments presented in the Petition in connection with Depetro and Choy likewise are materially different from the arguments presented to the Office in IPR252. For example, "Petitioner relies upon Depetro's teachings and its expert's testimony to assert that Depetro's transistor topology would *not* compromise ruggedness, unlike Williams's[6] transistor

[6] U.S. Patent No. 6,413,822 B2, issued July 2, 2002 (Ex. 1006). The challenge in IPR252 was based on a combination of references that included Williams. Paper 13, 4.

topology." *Id*. at 8 (citing Pet. 66 n.9 (citing Ex. 1004, 3:45–54; Ex. 1010 ¶ 124)). Unlike the Petition in IPR252, moreover, the instant Petition "explicitly addresses Williams's acknowledgement that increasing the effective area of the n+ source region reduces the ruggedness of the device, and explains that Depetro accounts for the potential reduction in ruggedness by introducing a strongly doped p+ region at the edge of the body." *Id*. at 6 (citing Pet. 66 n.9 (citing Ex. 1004, 3:45–54)).

On this record, we determine that the arguments presented in the Petition are not substantially the same as those previously presented in IPR252. Accordingly, we do not exercise our discretion to deny review under § 325(d). Pursuant to the Director's instructions, we next turn to the sufficiency of the challenges, as articulated in the Petition, to support institution of an *inter partes* review under § 314(a). *See id*. at 3 ("If the Board determines that it should not exercise its discretion to deny institution of *inter partes* review under § 325(d), then the Board should address the remaining issues raised in the Petition and Preliminary Response to determine whether to institute an *inter partes* review.").

E. Overview of the Asserted Prior Art

(1) Ryu

Ryu is titled "Vertical JFET Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors and Methods of Fabricating Vertical JFET Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors." Ex. 1003, code (54). Thus, Ryu relates to a metal-oxide semiconductor field effect transistor (MOSFET) that is formed on a silicon carbide substrate. *See generally*, Ex. 1003. Like the '633 patent, this prior art reference expressly is concerned with "high current, high voltage" power

MOSFETs. *Id.* ¶ 4; *see* Ex. 1001, 1:14–20 (explaining that the technical field of the invention of the '633 patent is power MOSFETs suitable for use in "high-voltage power applications").

We reproduce below Figure 2A from Ryu.

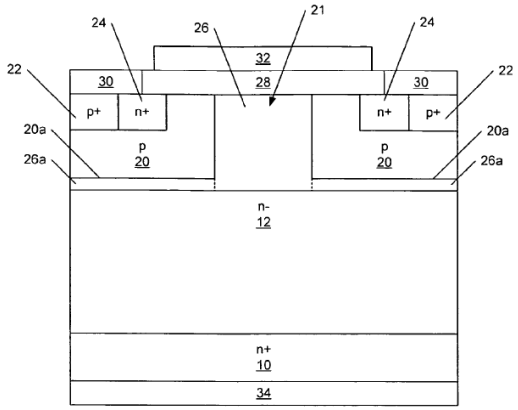


Figure 2A

Figure 2A is a cross-sectional view of a MOSFET according to the disclosure of Ryu that includes "an optional n^+ layer 10 of silicon carbide." Ex. 1003 ¶¶ 28, 40. Ryu explains that the device shown in Figure 2A "may be considered unit cells of devices having multiple cells." *Id.* ¶ 51.

Petitioner acknowledges that Ryu does not disclose the topside design of its source-region layout. Pet. 39. Petitioner contends that an ordinarily skilled artisan would have modified the MOSFET of Ryu's Figure 2A to include the source-region layout of Depetro or Choy. *Id.* at 40–41, 72–74.

(2) Depetro

Depetro is titled "DMOS Transistor Protected Against 'Snap-Back.'" Ex. 1004, code (54). Unlike the silicon carbide substrate of Ryu, Depetro's "transistor is formed on a monocrystalline silicon substrate." *Id.* at 1:17–19. Unlike Ryu's device, moreover, Depetro's device is described as a laterally diffused transistor. *Id.* at 1:10–20.

The challenge articulated in the Petition repeatedly and consistently directs the Board and Patent Owner to Depetro's Figure 1 as showing a topside source-region layout that, according to Petitioner, would have been included in the MOSFET of Ryu's Figure 2A. Pet. 40–41, 48, 51. We reproduce below Depetro's Figure 1.

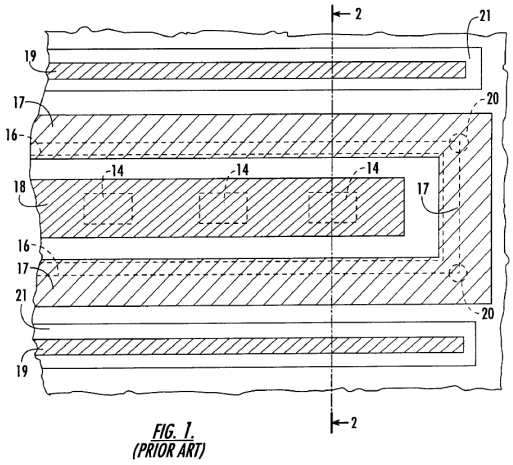


FIG. 1.
(PRIOR ART)

Figure 1 shows, in plan view, a portion of a prior art LDMOS, that is, a double-diffused metal-oxide semiconductor field-effect transistor. Ex. 1004, 1:10–11, 3:11–13.

(3) Choy

Choy is titled "Self-Aligned Structure and Process for DMOS Transistor." Ex. 1005, code (54). Choy relates to a transistor in which alternating n+ source regions and p++ body contact regions are positioned along the peripheries of overlapping gate structures. *Id.* at 3:32–37.

Petitioner directs the Board to Choy's Figure 3 as showing a topside source-region layout that, according to Petitioner, would have been included in the MOSFET of Ryu's Figure 2A. Pet. 38. We reproduce below Choy's Figure 3.

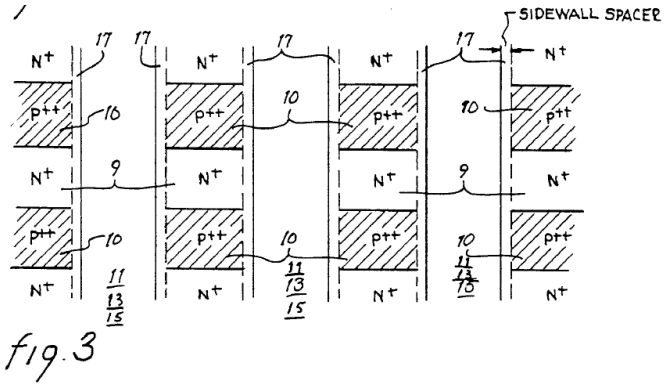
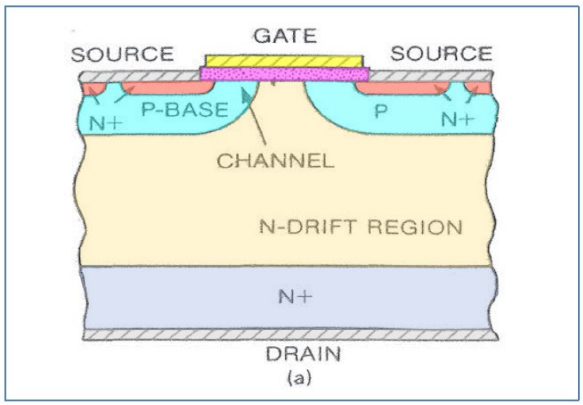


Figure 3 shows a top view of Choy's contact scheme for a transistor. Ex. 1005, 2:17–18.

F. Competing Considerations in MOSFET Design

A MOSFET is a device used for switching and regulating current in electronic circuits. Pet. 8 (citing Ex. 1010 ¶ 26). Power MOSFETs are designed for high-voltage and high-current applications. *Id.* (citing Ex. 1010 ¶ 27). We reproduce below an illustration, annotated by Petitioner, of "[a] conventional vertical power MOSFET." *Id.* (citing Ex. 1008, 265[7]).



The above figure is a "[c]ross-sectional view of the basic power MOSFET cell structures" for a semiconductor "fabricated by using planar diffusion

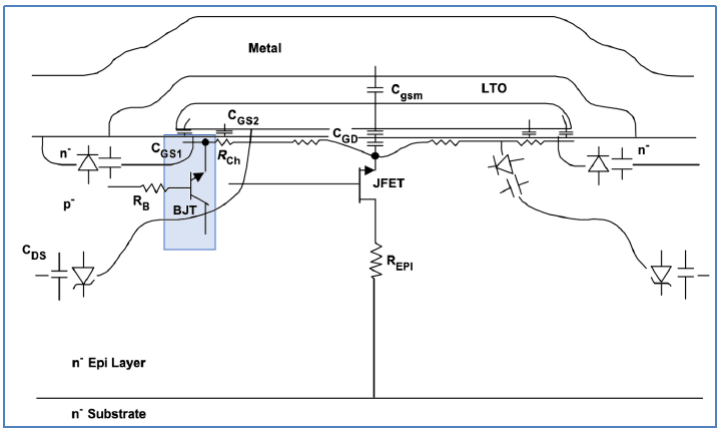
[7] B. Jayant Baliga, *Modern Power Devices*, by John Wiley & Sons, Inc. (1987).

technology." Ex. 1008, 264–265.[8] Petitioner uses color-shading to highlight components of the structure, identifying the "gate electrode (yellow), gate oxide (pink), upper source electrodes (gray), and lower drain electrode (gray)." Pet. 9. "Between the source and drain are a series of semiconductor layers, including an n+ substrate (blue), an n-type epitaxial drift layer (tan), p-type base regions (turquoise), and n+ source regions (red)." *Id.*

As Petitioner's witness, Dr. Lee, explains, in the on-state "of a vertical power MOSFET, the gate terminal is biased, which causes an electric field to form across the oxide layer." *Id.* at 10 (citing Ex. 1010 ¶ 30). In the off-state, by contrast, "the drift layer blocks any forward voltage applied to the device up to its breakdown voltage." *Id.* "A primary design concern, however, was large on-state resistance." *Id.* Petitioner identifies a number of different design techniques that were known to minimize on-resistance in power MOSFETs. *Id.* at 10–14. Those techniques would have been understood to come with trade-offs, however, and "[t]he most important design trade-off for power MOSFETs" at the time of the invention would have been "between on-resistance and breakdown voltage" affecting the ruggedness of the MOSFET. *Id.* at 10.

In particular, "[t]he inherent design of a MOSFET includes several parasitic components that can degrade performance." *Id.* at 14 (citing Ex. 1010 ¶ 38). "A key parasitic feature of power MOSFETs" of concern would have been "a bipolar junction transistor" or "BJT" component that may detrimentally turn on "between the source, body, and drain of the device." *Id.* The BJT phenomenon is depicted in the following illustration.

[8] We refer to original page numbers of exhibits, not pagination added by a party.



Pet. 14 (reproducing Ex. 1011, 10 (Figure 3.15)[9]). The above figure illustrates "[t]he origin of parasitic components within" a vertical diffusion metal-oxide semiconductor field effect transistor. Ex. 1011, 10–11. Petitioner annotates this figure to highlight, in blue shading, the parasitic BJT component between the source, body, and drain of the device. Pet. 14.

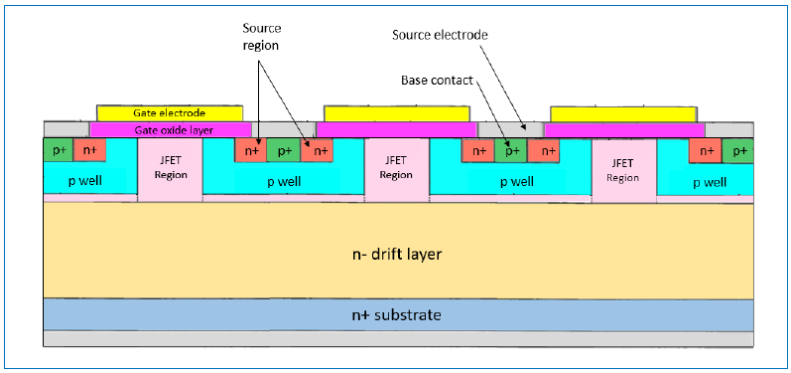
In addition to reducing on-resistance, therefore, "a known design consideration for power MOSFETs," which are designed for high-voltage and high-current applications, "was to prevent the" undesirable "parasitic transistor from turning on," which can result in "premature breakdown" of the device. *Id*. at 8, 15. Petitioner asserts that, at the time of the invention, "it was well known in the art that the design and doping concentration of the p+ region impacted" this consideration of "ruggedness" and the ability of the power MOSFET "to withstand turn-on of the parasitic bipolar transistor." *Id*. at 16 (citing Ex. 1010 ¶ 41; Ex. 1006, 16:28–35). For example, changing the relative areas of n+ and p+ regions affects the balance between on-resistance (which decreases with increasing the size of n+ regions) and breakdown voltage (which increases with decreasing size of p+ regions). Ex. 1006,

[9] Duncan A. Grant et al., *Power MOSFETS, Theory and Applications*, by John Wiley & Sons, Inc. (1989).

16:28–35, 17:15–19 (disclosures in Williams explaining these competing design considerations).

G. Sufficiency of the Challenge Based on Ryu and Depetro

Petitioner argues that the subject matter of claims 9–11 would have been obvious over Ryu and Depetro. Pet. 7, 63–69. Petitioner directs us to Figure 2A from Ryu for disclosure of a prior art power MOSFET having some of the limitations of the challenged claims. Pet. 39. We reproduce below Petitioner's modified and annotated version of Figure 2A from Ryu.

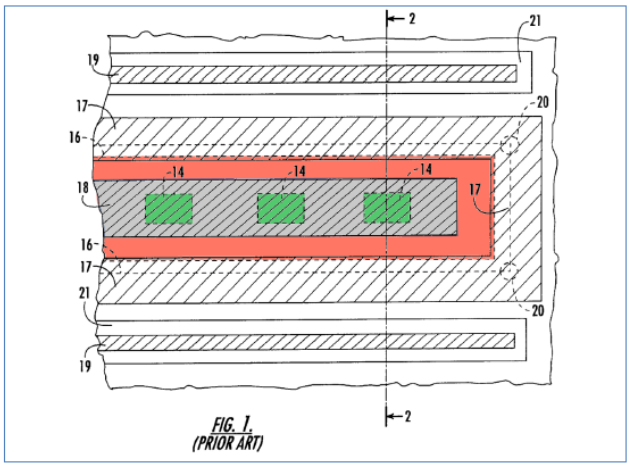


Pet. 39. The above figure illustrates elements of a power MOSFET when unit cells, as disclosed in Ryu's Figure 2A, are combined to "represent multiple cells in a single device." *Id*. Petitioner annotates the power MOSFET of Figure 2A to highlight in yellow the gate electrode, in magenta the gate oxide layer, in green the p+ base contact regions, in red the n+ source regions, in turquoise the p wells, in pink the JFET regions, in tan the n- drift layer, and in blue the n+ substrate.

We agree with Petitioner that Ryu suggests a power MOSFET having a preferred JFET region width of between about 1 and 10 microns, which overlaps the claimed ranges of less than about 3 microns (claim 9) or about 1 micron (claim 10). Pet. 60, 62; Ex. 1003 ¶ 44 (Ryu); Ex. 1001, 10:6–11 (JFET width limitations of claims 9 and 10). Petitioner acknowledges,

however, that Ryu does not disclose the topside layout of its n+ source regions or p+ base contact regions. Pet. 39. Petitioner relies on Depetro's teaching of a topside layout that includes p+ base contacts as "a plurality of spaced-apart islands" formed in the n+ source regions, where the "islands" are "defined along the longitudinal axis of the source electrode." *Id.* at 40.

To make out that limitation of the challenged claims, Petitioner relies on an annotated version of Depetro's Figure 1, which we reproduce below.



Pet. 40, 48, 51. Figure 1 illustrates, in plan view, a portion of a prior art lateral current conduction metal-oxide semiconductor transistor. Ex. 1004, 1:10–13, 3:11–12. Petitioner annotates Figure 1 to highlight in red shading n+ source regions and in green shading p+ contact base regions.

Critical to our analysis, Petitioner repeatedly indicates that the proposed combination supporting this challenge involves modifying Ryu's Figure 2A power MOSFET to include the source-region layout shown in Depetro's Figure 1. Pet. 3, 40–41, 47–49, 51–52, 57–58, 64–65.

In Patent Owner's view, Petitioner does not set forth sufficient non-hindsight-based reasons to combine the references in the manner claimed. Prelim. Resp. 43–49. In the next sections, we identify Petitioner's reasons

for the proposed combination, as set forth in the Petition, then assess whether those reasons are sufficient to support institution of review.

(1) Analogous Art

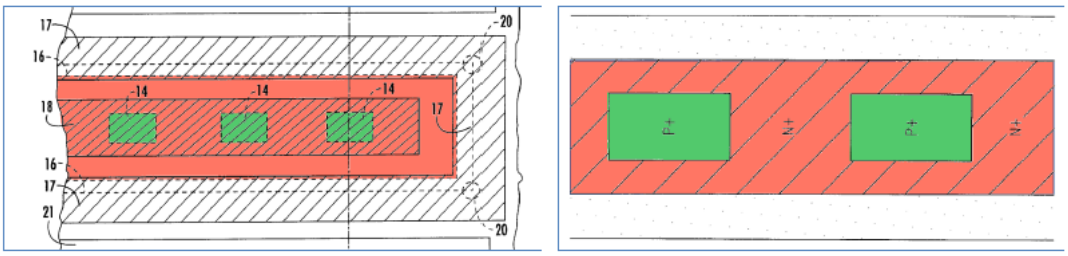
Petitioner submits that "Ryu and Depetro are analogous art to the claimed invention." Pet. 63. In Petitioner's view, these references and the claimed invention "are directed to MOSFETs for high-power applications" and, in particular, are pertinent to improved performance by reducing "on-resistance" while at the same time "preventing turn-on of the parasitic BJT to avoid premature breakdown" in high voltage applications. *Id*. On that basis, Petitioner argues that the ordinarily skilled artisan "would have looked to the teachings of Ryu and Depetro when considering how to improve the operation of high-power MOSFETs." *Id*.

(2) Applicability of Depetro's Source-Region Layout

Petitioner argues that an ordinarily skilled artisan "would have understood that the teachings of Depetro are directly applicable to the MOSFET of Ryu." *Id*. at 64. "When looking to improve the structure and operation of a double-implanted" silicon-carbide "device like Ryu," Petitioner contends, the ordinarily skilled artisan "would have looked to known double-diffused silicon devices like Depetro." *Id*. Specifically, according to Petitioner and its witness, Dr. Lee, that artisan would have sought out "designs that were known to improve performance metrics," which would have led to Depetro's source region layout because it was "known to reduce on-resistance while preventing turn on of the parasitic BJT." *Id*. (citing Ex. 1010 ¶ 121) (Dr. Lee's declaration testimony).

(3) Petitioner's Reliance on Williams

Petitioner argues that a background reference, Williams, would have provided a reason to modify Ryu's MOSFET to include the source-region layout of Depetro's Figure 1. Pet. 65. Petitioner, in that regard, asserts that Williams's Figure 19E "teaches the same source-region[] layout as" Depetro's Figure 1. *Id.* In support of that assertion, Petitioner advances a side-by-side comparison illustration, which we reproduce below.



Ex. 1004, Depetro at Fig. 1 Ex. 1006, Williams at Fig. 19E

Id. Petitioner's illustration compares the source-region layout of Depetro's Figure 1 (on the left) to the source-region layout of Williams's Figure 19E (on the right). Petitioner annotates both figures to highlight in green shading the p+ contact base regions, formed as islands in the n+ source regions, highlighted in red shading. Petitioner acknowledges that Depetro's Figure 1 "teaches the same source-region[] layout" as Williams's Figure 19E. *Id.*

Petitioner argues that a skilled artisan would have been led to modify the MOSFET of Ryu's Figure 2A to include the source-region layout of Depetro's Figure 1 because doing so would have been understood to reduce "the on-resistance of the resulting device, while preventing turn-on of the parasitic bipolar transistor and maintaining a high blocking voltage." *Id.* at 41 (citing Ex. 1010 ¶ 92). Petitioner's witness, Dr. Lee, repeats that assertion. Ex. 1010 ¶¶ 90, 92; *see id.* ¶ 121 (Dr. Lee's assertion that Depetro

"teaches a source-region layout known to reduce on-resistance while preventing turn on of the parasitic bipolar transistor").

In addition, Petitioner asserts that "it was well known in the art that the design and doping concentration of the p+ region impacted ruggedness of the device and its ability to withstand turn-on of the parasitic bipolar transistor." Pet. 16. Petitioner directs us to Dr. Lee's declaration, which repeats that assertion. *Id*. (citing Ex. 1010 ¶ 41). Dr. Lee and Petitioner rely on two supporting disclosures from Williams: First, that "[t]he design can be selected to maximize the N+ source perimeter (to achieve the lowest possible resistance) or to maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback, and ruggedize the device), or to compromise between the two;" and second, that the layouts of Williams's Figure 19E and 19F are "less rugged" than those of Williams's Figures 19A and 19B. *Id*. at 65 (citing Ex. 1006, 16:28–35, 17:15–19).

(4) Petitioner's Reliance on Nakayama

Nakayama teaches a source-region layout design that "is applicable in both silicon and [silicon carbide] devices." Pet. 68 (citing Ex. 1007 ¶ 45)[10]. Nakayama discusses parameters that suppress the increase in resistance "while at the same time permitting the stripe portions 4 a of source layer 4 to stay smaller in width." *Id*. (quoting Ex. 1007 ¶ 57). According to Nakayama, on that basis, "it is possible to achieve high-reliability electrical contact of the short electrode 9 with the source layer 4 while retaining enhanced avalanche ratings." *Id*. We reproduce below Figure 11 from Nakayama,

[10] US 2004/0046202 A1, pub. Mar. 11, 2004 (Ex. 1007). Petitioner misidentifies Nakayama as Exhibit 1005. Pet. 68. We use the correct designation, which is Exhibit 1007.

which Petitioner advances as illustrating "the same source-region geometry as Depetro." *Id*. at 67.

FIG. 11

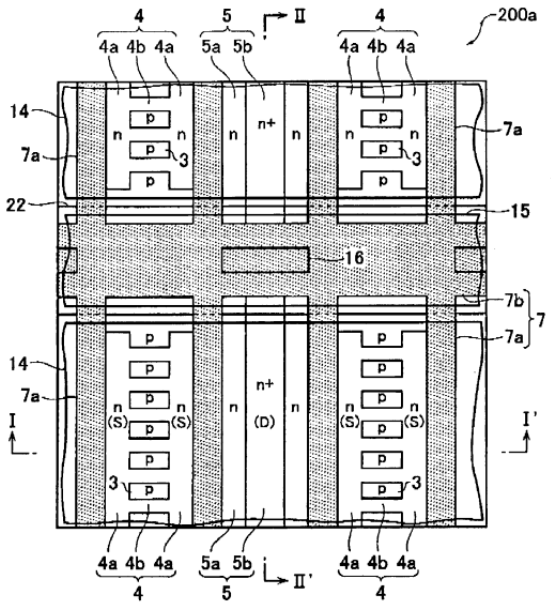


Figure 11 from Nakayama is "a plan view of [a] main part of a MOSFET." Ex. 1007 ¶ 25.

(5) Finite Number of Design Choices

Petitioner submits that there would have been a finite number of source-region layouts known in the art. On that basis, Petitioner argues that it would have been a routine matter to try all of them to attain the claimed invention. Pet. 68–69.

(6) Analysis of the Articulated Reasons to Combine

We next resolve whether Petitioner shows sufficiently that an ordinarily skilled artisan would have modified the MOSFET of Ryu's Figure 2A to include the source-region layout of Depetro's Figure 1. Pet. 39–62 (repeatedly and consistently advancing those two figures from the prior art as the combination that supports this ground).

Petitioner acknowledges that Williams's Figure 19 E "teaches the same" source-region layout as Depetro's Figure 1. Pet. 65 (including comparison illustration). Petitioner also acknowledges that the layout of Depetro's Figure 1, just like the layout of Williams's Figure 19E, decreases on-resistance (by increasing the n+ source region) but *sacrifices ruggedness* (by decreasing the p+ base contact region) to achieve the highest possible reduction in on-resistance. Pet. 66 n.9; *see* Ex. 1006, 1:60–61, 16:28–35, 17:15–19. Specifically, as Petitioner points out, "the tradeoff for increasing the effective area of the n+ source region," as in Depetro's Figure 1 and Williams's Figure 19E, is a "reduction in ruggedness" of the MOSFET. Pet. 66 n.9 (citing Ex. 1006, 16:28–35); *see* Ex. 1006, 1:50–52 ("The primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents"), 1:60–61 ("There is an unavoidable tradeoff between the avalanche breakdown voltage and the on-resistance of the device.").

Petitioner further acknowledges that "the trade-off for increasing the effective area of the n+ region," as in the layout of Williams's Figure 19E or Depetro's Figure 1, "is a reduction in ruggedness of the device," but proposes that this "would not dissuade" the ordinarily skilled artisan "from adopting spaced apart p+ regions" formed as islands in the n+ source region. Pet. 66 n.9; *see* Ex. 1004, Fig. 2, 2:4–16 (Depetro's teaching that the source-region layout of Figure 1 is prone to "snap-back," a phenomenon that "considerably limits the field of use of the transistor" due to "switching-on of" the parasitic bipolar transistor). Specifically, in support of that proposition, Petitioner argues that an ordinarily skilled artisan "would have

recognized that the design can be balanced by adjusting the size and doping concentration of the p+ regions." Pet. 66 n.9 (citing Ex. 1010 ¶ 124).

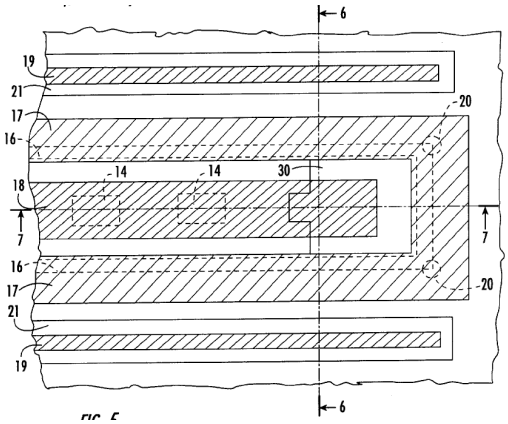
On that point, both Petitioner and Dr. Lee direct the Board to a disclosure from Depetro that describes a layout which "accounts for the potential reduction in ruggedness by introducing a strongly doped p+ region at the edge of the body." Pet. 66 n.9 (citing Ex. 1004, 3:45–54). We reproduce below the cited disclosure from Depetro:

> With reference to FIGS. 5, 6, and 7, in which parts identical or corresponding to those of the known transistor shown in FIGS. 1 and 2 are indicated by the same reference numerals. According to the invention, a strongly doped p-type region, indicated 30, is associated with the corners 20 of the elongate body region. This region 30 extends into the body region 12 taking the place of the end portion of the n source region 13 of the known transistor of FIGS. 1 and 2 and is in surface electrical contact with the second electrode 18.

Ex. 1004, 3:45–54; *see* Ex. 1010 ¶ 124 (Dr. Lee, repeating *verbatim* Petitioner's argument about this disclosure from Depetro).

We agree with Petitioner that this disclosure describes Depetro's solution for balancing the tradeoff between on-resistance reduction and parasitic turn-on prevention. Ex. 1004, 1:16. But this disclosure does not describe the "conventional" layout of Figure 1: It pertains to a different embodiment, illustrated in Figures 5, 6, and 7, having features that address the snap-back problem that plagues the conventional Figure 1 layout. *Id.* at 1:14–20, 1:61–2:39, 3:30–65.

We reproduce below Figures 5, 6, and 7 from Depetro.



Ex. 1004, Fig. 5.

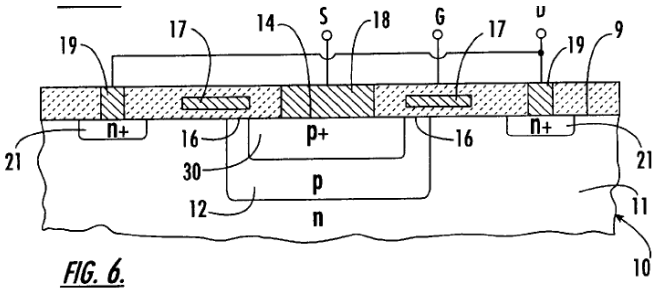


FIG. 6.

Ex. 1004, Fig. 6.

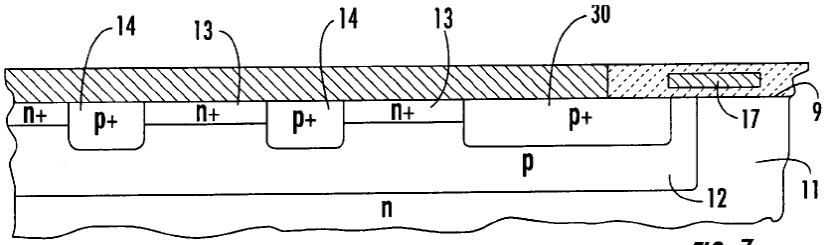


FIG. 7.

Ex. 1004, Fig. 7. Figures 5, 6, and 7 together illustrate Depetro's solution to the snap-back problem that occurs in high-voltage applications; a solution that, in contrast to the conventional layout of Figure 1, includes "a strongly doped p-type region," identified as element 30, which "is associated with the corners 20 of" elongate

body region 12, "extends into" elongate body region 12 and takes "the place of the end portion of" n+ source region 13. *Id*. at 3:45–54.[11]

In a nutshell, Petitioner and Dr. Lee rely on a disclosure from Depetro that does not support a rationale for selecting Depetro's Figure 1 layout for inclusion in the MOSFET of Ryu's Figure 2A. Pet. 66 n.9; Ex. 1010 ¶ 124 (both citing Ex. 1004, 3:45–54). To the contrary, the cited disclosure indicates that the embodiment of layout of Depetro's Figures 5, 6, and 7 — but not the "conventional" layout of Figure 1 — incorporates the solution of a strongly doped p+ region to address the "snap back" that "considerably limits the field of use of" a power MOSFET having the "conventional" source region layout of Depetro's Figure 1. Ex. 1004, 1:14–20, 1:61–2:39, 3:30–65.

As Patent Owner points out, the challenge articulated in the Petition repeatedly and consistently identifies Depetro's conventional Figure 1 layout as the source-region layout proposed for combination with Ryu's power MOSFET. *See* Paper 8, 2 (citing Pet. 39–63, 66 n.9). Depetro unequivocally explains, however, that the conventional Figure 1 layout, which does *not* include the strongly doped p+ regions described in Figures 5, 6, or 7, would have experienced "snap-back" that limits the utility of the design in high-voltage applications such as those described in Ryu. Ex. 1004, 1:17, 2:11–13. We take no position on whether the disclosure from Depetro advanced by Petitioner and

[11] Depetro's Figures 5, 6, and 7 describe a layout that replaces some of the n+ region with p+ region, a modification that desirably increases the parasitic turn-on voltage (by increasing the p+ region) but also necessarily and detrimentally increases on-resistance (by decreasing the n+ region). *See supra* 15–18 (explaining those competing design considerations).

Dr. Lee would support a rationale for selecting the source-region layout of Figures 5, 6, or 7 for use in Ryu's power MOSFET. Constrained by the record before us, it is enough for us to observe that the relied-upon disclosure does *not* support a reason for selecting the "conventional" layout of Figure 1. Ex. 1004, 1:15–17; *see* Pet. 66 n.9; Ex. 1010 ¶ 124 (both citing Ex. 1004, 3:45–54, reproduced *supra* 25).

This case presents a close question as to whether Petitioner, in the Petition, places Patent Owner on fair notice that the challenge is based on modifying Ryu's Figure 2A MOSFET to include the source-region layout described in Depetro's Figure 5, 6, or 7, as opposed to the conventional layout described in Depetro's Figure 1. We answer that question in the negative because Petitioner repeatedly reproduces and exclusively cites to Depetro's Figure 1 when mapping the prior art to the limitations of the challenged claims, and never once refers to Depetro's Figure 5, 6, or 7 when identifying the prior art combination that forms the basis for the challenge. Pet. 39–63; *see especially id.* at 40–41, 48, 51 (decisive argument that Depetro's Figure 1 source-region layout is the embodiment advanced in the challenge for modification of Ryu's Figure 2A power MOSFET).

We acknowledge that Petitioner, in a footnote that appears in a section of the Petition devoted to the reasons to combine the references, alludes to an embodiment of Depetro's source-region layout that includes the strongly doped p+ region of Figures 5, 6, and 7, but ultimately, we agree with Patent Owner that the Petition does not set forth a ground based on those figures with the clarity or particularity required to support institution of review. Paper 8, 2

(citing Pet. 39–63, 66 n.9). "Instead, the Petition consistently point[s] to Depetro's Figure 1 source-region layout, ***without*** a strongly doped p+ region," as "being 'applied to the DIMOSFET of Ryu.'" *Id.* (quoting Pet. 40; citing *id.* at 3, 41, 47–49, 51–52, 57–58, 64–65) (Patent Owner's emphasis).

In our forum, a petitioner "has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc.*, 815 F.3d at 1363. Accordingly, a petition for *inter partes* review must identify "with particularity," by reference to the record, "the evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3). Petitioner, in the Petition, does not identify with particularity a challenge based on modifying Ryu's Figure 2A MOSFET to include the source-region layout shown in Depetro's Figure 5, 6, or 7. Pet. 38–63 (when articulating the proposed combination of prior art, mapping claim limitations exclusively to embodiments shown in Ryu's Figure 2A and Depetro's Figure 1).

In reaching that determination, we take account of Petitioner's citation to a disclosure in Depetro that relates to the source-region layout of Figures 5, 6, and 7, but that citation is in a footnote that pertains only to the rationale to combine Ryu's Figure 2A power MOSFET with Depetro's Figure 1 layout. Pet. 66 n.9; *compare id.* at 38–63 (statement of challenge, nowhere articulating a ground based on Depetro's Figure 5, 6, or 7).

We observe that Petitioner reproduces Depetro's Figure 5 in a section of the Petition that describes the prior art (Pet. 36), but find that background section insufficient to place Patent Owner on notice that the challenge is based on the Figure 5 layout, where the challenge itself relies exclusively on the Figure 1 layout. *See id.* 38–63 (statement of the challenge, including

claim mapping, nowhere referring to Depetro's Figure 5, 6, or 7 and consistently reproducing and relying on Depetro's Figure 1); *see id*. at 57 (single occurrence of Petitioner's reliance on Depetro's Figure 2, which is a section taken on the line II–II of Depetro's conventional Figure 1 layout (Ex. 1004, 1:15–17, 3:13)).

We are disinclined to rewrite the challenge, as articulated in the Petition, to include a ground based on the combination of Ryu's Figure 2A MOSFET with the source-region layout of Depetro's Figures 5, 6, or 7. *See* Pet. 39–63 (Petitioner's explanation of the combination that forms the basis for this ground, which plainly rests on modifying Ryu's Figure 2A MOSFET to include Depetro's Figure 1 source-region layout). Doing so would violate binding precedent of our reviewing court. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380–81 (Fed. Cir. 2016) (instructing that the Board cannot adopt arguments on behalf of petitioners or raise obviousness arguments not asserted in a petition) (citations omitted).

Alternatively, we find that Petitioner is not likely to prevail at trial with respect to at least one challenged claim because the challenge, as articulated in the Petition, repeatedly relies on a facially incorrect factual proposition that Depetro's Figure 1 layout would *not* have sacrificed ruggedness in a high-voltage application such as Ryu's power MOSFET. Pet 64 (advancing Williams to support that incorrect proposition in connection with this rationale); *see id*. at 3, 14, 16, 19, 65, 66 n.9, 69 (advancing Williams to assert that same incorrect proposition); *compare* Ex. 1004, 2:11–34 (Depetro's clear explanation of the limited utility of the Figure 1 layout in preventing snap-back in high-voltage applications).

Petitioner raises additional reasons for the proposed combination but none compensates for the deficiencies described above. For example, Petitioner submits that an ordinarily skilled artisan would have been aware of Ryu and Depetro because they "are analogous art to the claimed invention." Pet. 63. The question of whether the prior art references are in the same field of endeavor is merely a jumping-off point in the determination of whether a claimed invention is obvious. *See K-Tec, Inc. v. Vita-Mix Corp.*, 696 F.3d 1364, 1375 (Fed. Cir. 2012) (to qualify as prior art in an obviousness analysis, references must be analogous art—either in the same field of endeavor, or reasonably pertinent to the problem with which the inventor is involved).

Petitioner also submits that Depetro's Figure 1 layout would have been understood to reduce "on-resistance by increasing the effective area of the n+ source regions," but that circumstance does not move the needle much, where there is no dispute on this record that an ordinarily skilled artisan would have been driven to balance reduced on-resistance against the competing design goal of suppressing turn-on of the parasitic bipolar transistor. Pet. 66 n.9. Petitioner does not address adequately why Depetro's Figure 1 layout, which sacrifices ruggedness, nonetheless would have been selected for inclusion in Ryu's MOSFET design in view of that goal. Pet. 64; *see id.* at 66 n.9 (failing to explain that position adequately); Ex. 1006, 16:28–35 (Williams's disclosure on that point).

It bears repeating that Petitioner does not meaningfully dispute that balancing those competing design considerations would have been a primary concern at the time of the invention; indeed, attaining that balance is the

focus of the '633 patent and necessary "to avoid premature breakdown" of a power MOSFET such as Ryu's. Ex. 1010 ¶ 120 (Petitioner's witness, Dr. Lee, citing Ex. 1001, 1:18–36); *see* Section III(F), *supra* 15–18; *see also* Pet. 10, 14–17; Ex. 1010 ¶¶ 31, 38 (additional support for this finding).

The technical field of the invention of the '633 patent, as well as the particular subject matter of Ryu, is power MOSFETs used in "high-voltage power applications." Ex. 1001, 1:14–20; *see* Ex. 1003 ¶ 4 (explaining that Ryu likewise is concerned with "high current, high voltage" power MOSFETs). Against that backdrop, Petitioner identifies the impetus behind the selection of a source-region layout for use in Ryu's power MOSFET as the desire "to balance the design considerations" of "low on-resistance and preventing turn-on of the parasitic BJT to avoid premature breakdown." Pet. 18–19. On this record, including Petitioner's repeated reliance on a facially incorrect proposition that Depetro's Figure 1 layout would *not* have sacrificed ruggedness in high-voltage applications, we examine the Petition for a non-hindsight-based "reason that would have prompted a person of ordinary skill in the relevant field to combine elements in the way the claimed new invention does," but find none. *KSR*, 550 U.S. at 418.

For example, Petitioner argues that, when modifying Ryu's power MOSFET, it would have been obvious to try all of the source-region layout designs that would have been available to the ordinarily skilled artisan at the time of the invention. Pet. 68–69. Based on the knowledge that Depetro's Figure 1 layout would have sacrificed ruggedness in high-voltage applications, under the particular circumstances presented in this case, that argument is not tethered adequately to the undisputed impetus behind the selection, namely, the desire "to balance the design considerations" of "low

on-resistance and preventing turn-on of the parasitic BJT to avoid premature breakdown." Pet. 18–19. For that reason, we detect in this argument the unmistakable taint of impermissible hindsight reconstruction.

Petitioner also observes that Nakayama teaches "the same source-region geometry as Depetro, with p-type contact regions spaced apart in the n-type source regions," and would have been understood to reduce on-resistance, but that is nothing new over the disclosures of Williams and Depetro. *Id*. at 67 (citing Ex. 1007 ¶ 5); *see id*. at 20 (for assertion that Nakayama teaches the known benefit of reducing on-resistance"); *see also* Ex. 1006, 16:28–35 (Williams's teaching that a source-region layout design "selected to maximize the N+ source perimeter" will "achieve the lowest possible resistance"). Petitioner does not explain adequately how or why Nakayama provides a rationale for selecting the layout of Depetro's Figure 1 for inclusion in Ryu's power MOSFET. *See* Pet. 39–63 (consistently advancing the combination of Depetro's Figure 1 and Ryu's Figure 2A).

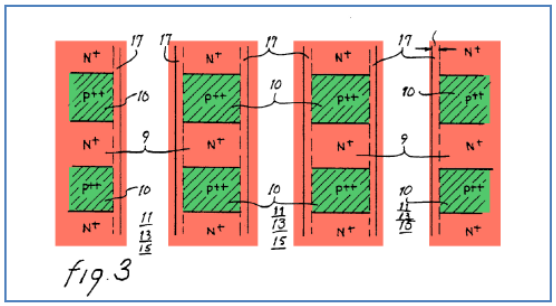
For the above reasons, constrained by the record before us, we determine that Petitioner is not reasonably likely to prevail in showing that the subject matter of at least one challenged claim is unpatentable based on the ground that asserts Ryu and Depetro. Specifically, the Petition does not articulate "reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (citation omitted).

H. Sufficiency of the Challenge Based on Ryu and Choy

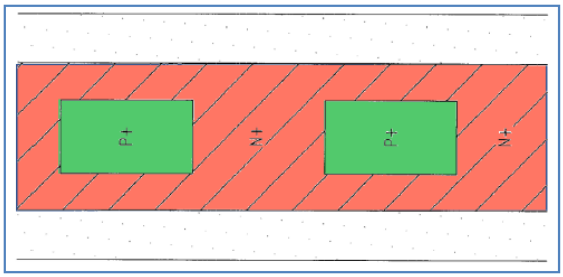
Petitioner also asserts that claims 9–11 are unpatentable as obvious over the combined disclosures of Ryu and Choy. Pet. 7. Petitioner argues that an ordinarily skilled artisan would have been led to modify Ryu to include the source-region layout of Choy, so that p+ base contacts are

"formed in the n+ source region [] as a plurality of spaced-apart islands." *Id.* at 73. In particular, Petitioner directs us to the topside source-region layout depicted in Choy's Figure 3, reproduced *supra* 15.

When addressing the reasons to combine Ryu and Choy, however, Petitioner advances essentially the same arguments about Choy as are asserted in connection with Depetro. *Compare* Pet. 64–69, *with id.* at 88–91. For example, Petitioner argues that Williams's Figure 19E "teaches the same source-region[] layout as Choy" and, by way of support, provides the following side-by-side illustration that compares those two figures.



Ex. 1005, Choy at Fig. 3



Ex. 1006, Williams at Fig. 19E

Pet. 90. The above illustration compares Choy's Figure 3 (on the left) and Williams's Figure 19E (on the right). Both show the topside geometry of a source-region layout for a transistor. Petitioner adds highlighting to both figures to shade in green the p+ regions and in red the n+ regions.

Our reasoning regarding Petitioner's articulated reasons to combine Ryu and Depetro apply with equal force to the proposed combination of Ryu and Choy. *Compare* Pet. 64–69, *with id.* at 88–91 (showing that Petitioner raises substantially the same arguments in connection with both grounds). In particular, Petitioner directs us to evidence—a disclosure from Williams and a portion of Dr. Lee's declaration testimony—that is insufficient to support Petitioner's statement that the source-region layout of Choy's Figure 3,

which is "the same" as the layout of Williams's Figure 19E, would have been understood to improve on-resistance "without sacrificing suppression of the parasitic bipolar transistor." *Id*. at 90 (citing Williams, Ex. 1006, 16:28–35, 17:15–19, and Dr. Lee's testimony, Ex. 1010 ¶ 166).

Accordingly, based on the information presented, we determine that the reasons for the proposed combination of Ryu and Choy, as articulated in the Petition, are insufficient to support institution of review. We determine, therefore, that Petitioner does not show a reasonable likelihood of prevailing at trial with respect to at least one challenged claim based on the ground that asserts Ryu and Choy.

IV. CONCLUSION

For the above reasons, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing with respect to at least one claim. Accordingly, pursuant to § 314(a), we deny the Petition and do not institute an *inter partes* review.

V. ORDER

It is

ORDERED that the Petition is denied and no *inter partes* review is instituted.

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